LOW-COST RELIABLE ONBOARD COMPUTER FOR SMALL SATELLITES

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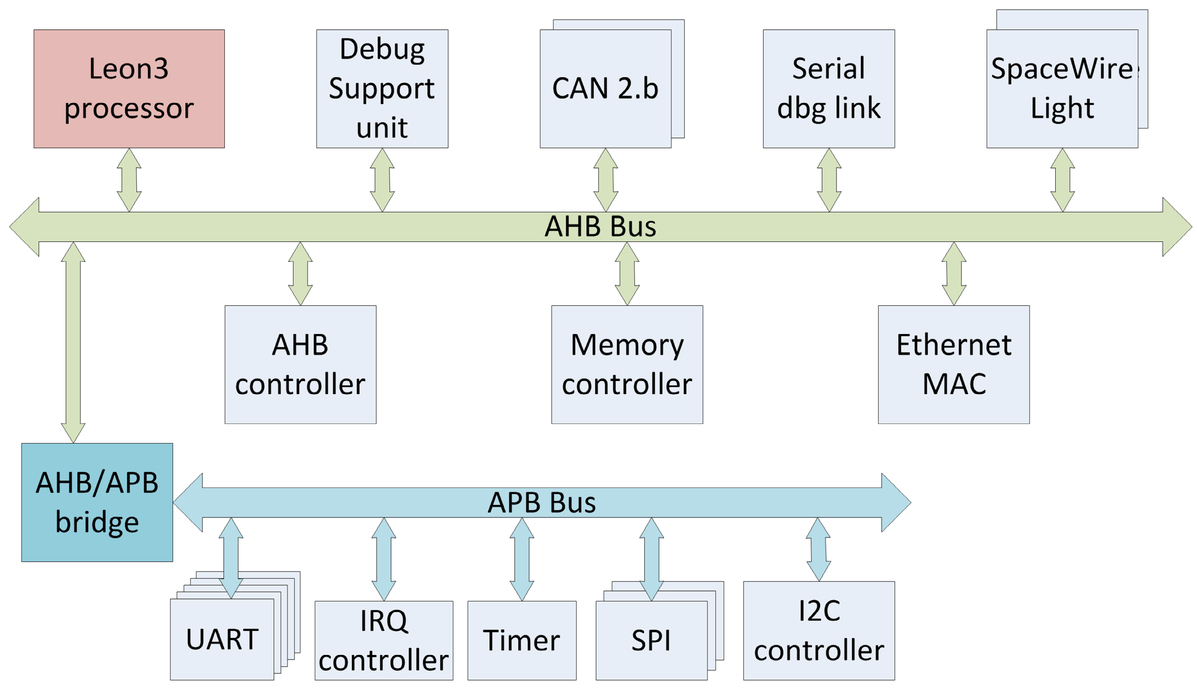
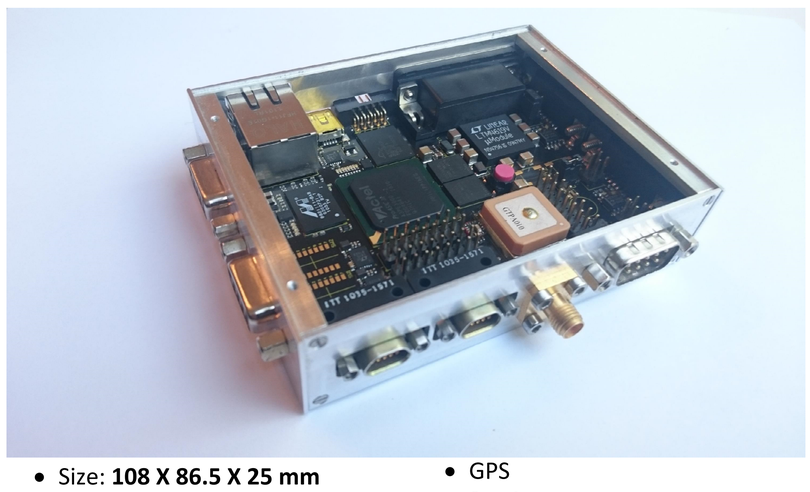
ABSTRACT

The market of Small Satellites (SS) is rapidly growing. Many SS projects use industrial grade COTS components instead of space and military grade ones in order to significantly minimize the costs. Low tolerance to radiation is known to be the main issue of electronics based on industrial grade components. We have designed a low-cost and reliable onboard computer (OBC) for low Earth orbit (LEO) missions. The computer architecture is based on LEON3FT processor core implemented inside FPGA. The OBC utilizes special multichannel guard system to prevent impact of destructive Single Event Effects (SEE) such as Single Effect Latchup (SEL). TID tests performed on our OBC showed the level of parametric degradation of the most susceptible components to be above 10 krads. Designed solutions along with using 3mm aluminum shielding would allow the OBC to operate in LEO for more than 5 years.

SOC inside Actel FPGA



OBC (revision A)



- Size: **108 X 86.5 X 25 mm**
- Mass: **0.2 kg**
- Power supply : **5 to 25 V**
- Power consumption: **1.2 W**
- Performance: **25 MIPS**
- RAM: **16 Mb** (SRAM)
- ROM: **64 Mb** (FLASH)
- GPS
- 3-axis gyro
- 3-axis accelerometer
- Interfaces: **SpaceWire,**
- **CAN 2.b, Ethernet, RS232, RS422, SPI, M-LVDS**

Testing and validation

The most important stage of the designing flight equipment is preflight tests. Full cycle of tests and experiments was performed on onboard computers for confirming the quality and compliance to technical tasks. The list of conducted tests is presented below:

1. X-ray control for checking quality of manufacturing
2. Functional tests
3. Thermocyclic tests
4. Vacuum tests
5. Vibration tests.
6. Radiation tests

Conducting functional tests during thermocyclic testing and vacuum testing allows simulating onboard operation process in close to orbital conditions. This method shows weak points in design and emphasizes the right solutions.

Hybrid OBC (revision B)

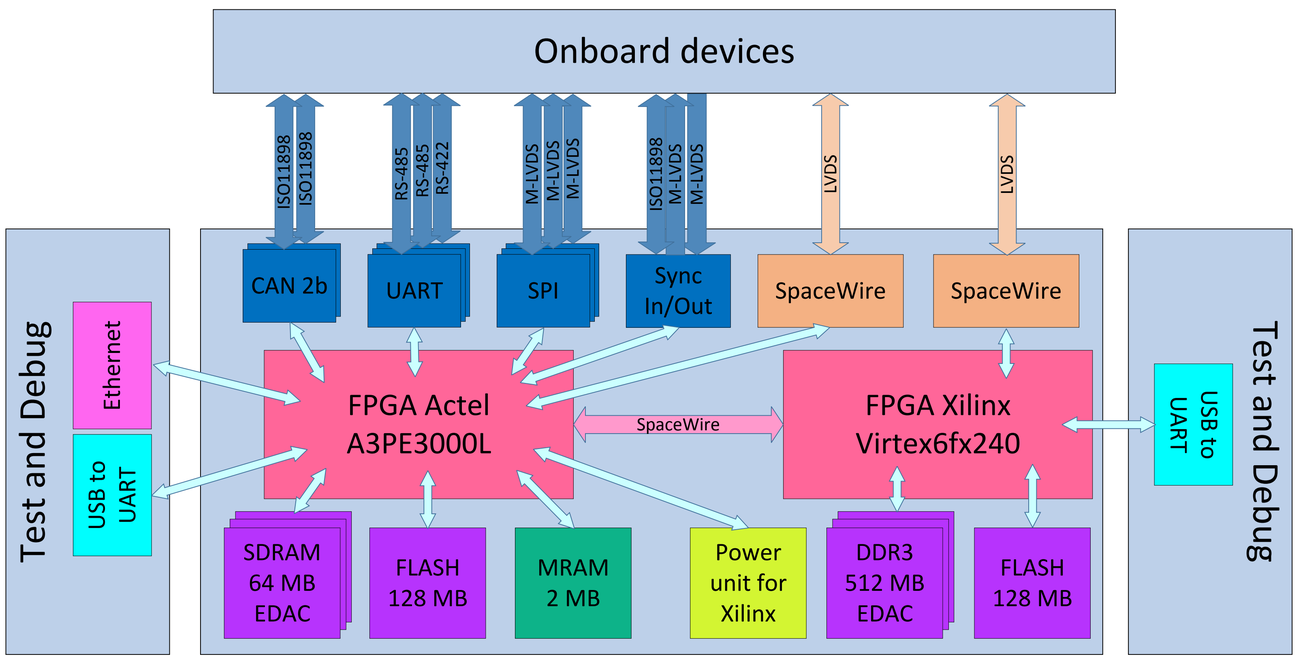
Hybrid OBC is built on two different cores. The first core is reliable and its architecture is similar to OBC revision A. The second one is a high-performance core for high-speed processing of special tasks. This core is controlled by the reliable core and may be deactivated for saving energy. Communication between cores is organized on SpaceWire interface.

High-reliability core based on Actel ProASIC3E FPGA Protected from SEU

- Power consumption 1W
- Speed 26 MIPS
- RAM SDRAM 64 MB + 32 MB EDAC
- ROM: FLASH 64 MB + 64 MB EDAC
- MRAM: 1 MB + 1 MB EDAC
- Interfaces: 2x CAN 2.0B, 2x RS485, RS422, 3x SPI (M-LVDS)

High-speed core based on Xilinx Virtex-6 FPGA

- Power consumption 7W
- Speed ~300000 MAC
- RAM DDR3 512 MB + 256 MB EDAC
- ROM: FLASH 128 MB
- Interfaces: CAN 2.0B, SpaceWire, M-LVDS, Time sync



Conclusion

Methods and engineering solutions utilized in both revisions of OBC give an opportunity to make a huge step forward in designing low-cost equipment with extremely high reliability. Based on previous OBC designs, which MIPT currently improves and upgrades, MIPT works on new revision of redundant OBC which consist of two similar subsystems. Each subsystem is a completed OBC. This duplicated configuration can operate in hot or cold redundancy mode. If consider the probability of no-failure operation equal to 0.997, duplicated solution increases redundancy by more than 20 times while costs of manufacturing rise just twice. This solution and continuously developing methods of radiation hardening will allow building an OBC for the highest LEO with operation time up to 10 years.